UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/883,681	06/18/2001	Ashok Singhal	M-8496 US	1044

32566 7590 06/03/2004

PATENT LAW GROUP LLP
2635 NORTH FIRST STREET
SUITE 223
SAN JOSE, CA 95134

EXAMINER	
PATEL, NIMESH G	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/883,681	SINGHAL ET AL.	
	Examiner	Art Unit	
	Nimesh G Patel	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 3-16, and 18-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-16 and 18-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 19 is objected to because of the following informalities: Claim 19 recites "in a second type of data transfer," but there is no first type of data transfer. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 24 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 24 recites the limitation "said burdening" in line 1 of claim 24. There is insufficient antecedent basis for this limitation in the claim. Also, the claim is unclear as to what the burdening the computer-memory complex means.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, and 3-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Cohen('464).

7. Regarding claim 1, Cohen discloses a node controller(Figure 1, 18) for a data storage system having at least one node for providing access to a data storage facility(Figure 1, 30), the node controller distinct from a computer-memory complex, the node controller providing overall control for transferring data through the node. Cohen further discloses a node controller comprising a logic engine operable to perform a logic operation on data from at least one data source in the data storage system(Column 6, Lines 5-7; Figure 3, 56; It is inherent an address comparator performs logic operations on address data).

8. Regarding claim 3, Cohen discloses a node controller, wherein at least one data source is one of an interconnect link, a peripheral component interconnect (PCI) bus, or a cluster memory(Figure 1).

9. Regarding claim 4, Cohen discloses a node controller, wherein the logic engine comprises an exclusive OR engine(Column 6, Lines 5-7; Figure 3, 56; It is inherent that address comparators use exclusive OR engines, as evidenced by Malinowski('441)).

10. Regarding claim 5, Cohen discloses a node controller comprising a command queue operable to store a logic control block to be processed by the logic engine(address comparator), the logic control block(transaction) specifying said at least one data source(Column 5, Lines 24-43; The address specifies the data source).

11. Regarding claim 6, Cohen discloses a node controller comprising a memory controller(Figure 3, 58) operable to interface with a cluster memory(Figure 1, 20).

12. Regarding claim 7, Cohen discloses a node controller, wherein the node controller is implemented as an integrated circuit device(Figure 1, 18).

13. Regarding claim 8, Cohen discloses a node controller comprising a peripheral component interconnect (PCI) control interface operable to support an interface between the node controller and a PCI bus(Column 5, Lines 13-23).

14. Regarding claim 9, Cohen discloses a node controller comprising a logic engine operable to perform a logic operation on data from at least one data source in the data storage system(Column 6, Lines 5-7; Figure 3, 56; It is inherent the address comparator performs logic operations on the address data) and a command queue coupled to the logic engine, the command queue operable to store a logic control block which can be processed by the logic engine(Column 5, Lines 24-43).

15. Regarding claim 10, Cohen discloses a node controller wherein the at least one data source is one of an interconnect link, a peripheral component interconnect (PCI) bus, or a cluster memory(Figure 1).

16. Regarding claim 11, Cohen discloses a node controller, wherein the logic engine comprises an exclusive OR engine(Column 6, Lines 5-7; Figure 3, 56; It is inherent that address comparators use exclusive OR engines, as evidenced by Malinowski('441)).

17. Regarding claim 12, Cohen discloses a node controller comprising a memory controller(Figure 3, 58) operable to interface with a cluster memory(Figure 1, 20).

18. Regarding claim 13, Cohen discloses a node controller, wherein the node controller is implemented as an integrated circuit device(Figure 1, 18).

19. Regarding claim 14, Cohen discloses a node controller a peripheral component interconnect (PCI) control interface operable to support an interface between the node controller and a PCI bus(Column 5, Lines 13-23).

20. Regarding claim 15, Cohen discloses a node controller wherein the node controller is operable to be programmed by the computer-memory complex(the computer-memory complex would have to initialize the node controller and therefore would have to "program" the controller).

21. Regarding claim 16, Cohen discloses a producer register operable to specify a first address of the command queue and a consumer register operable to specify a second address of the command queue (Column 5, Lines 24-43).

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

24. Claims 18-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen, in view of Styczinski('860).

25. Regarding claim 18, Cohen discloses a node controller comprising: a plurality of input/output interfaces for coupling to a plurality of buses, where in the buses are coupled to a computer-memory complex of the node and each bus can be coupled to a plurality of devices(Column 5, Lines 21-23); a memory controller(Figure 3, 58) for coupling to memory and a backplane, wherein the backplane can be coupled to a plurality of other node controllers in the data storage system(It is inherent for modern systems to have backplanes to connect devices).

Cohen does not specifically disclose a plurality of command queues. However, Styczinski discloses a plurality of command queues(Write service queue, WAD queue). Therefore, it would have been obvious to combine the teachings of Styczinski in the system of Cohen, since it is common to have each bus have its own queue for transactions in the node controller.

Styczinski further discloses a plurality of command queues storing logic control blocks each defining a logic operation to be performed by a logic engine, a plurality of data sources for the logic operation and a data destination for a result of the logic operation(Column 8, Line 48-Column 9, Line 10); wherein the logic engine performs the logic operation to a plurality of data from the plurality of data sources and writes the result of the logic operation to the data destination, each of the plurality of data sources being selected from the group consisting of one region in the memory and one of the devices, the data destination being selected from the group consisting of one region in the memory, one of the devices, and one of the other node controllers(Column 8, Line 48-Column 9, Line 10).

26. Regarding claim 19, Styczinski discloses a node controller, wherein, in a second type of data transfer, a data source(Figure 1, 101) writes a data into the memory and in response the logic engine copies the data to at least one data destination(Figure 1, 105), the data source being selected from the group consisting of one of the devices and one of the other node controllers, the data destination being selected from the group consisting of one region in the memory, one of the devices and one of the other node controllers(Column 8, Line 48-Column 9, Line 10).

27. Regarding claim 20, Styczinski discloses a node controller, wherein each of the devices is selected from the group consisting of a host device(Figure 1, 101) and a data storage device(Figure 1, 105).

28. Regarding claim 21, Cohen discloses a node controller, wherein each of the input/output interfaces comprises a peripheral component interconnect(PCI) controller and each of the buses comprises a PCI bus(Figure 1, 36).

29. Regarding claim 22, Styczinski discloses a node controller, wherein the computer-memory complex mages the PCI bus(It is inherent the PCI bus is managed by the computer-memory complex).

30. Regarding claim 23, Cohen and Styczinski do not specifically disclose a node controller wherein the computer-memory complex supports a service selected from the group consisting of a HTTP service, a NFS service, and a CIFS service. Examiner is taking official notice that these services are well-known in the art(HTTP is used for internet, NFS is a standard used for providing file system mounts among Unix systems, and CFSI is the new proposed standard for an Internet File System) and would be obvious to use the computer-memory complex for such services since these services use a network of computers or nodes.

31. Regarding claim 25, Styczinski discloses a node controller, wherein the logic operation comprises an XOR operation(Column 5, Lines 35-38).

32. Regarding claim 26, Styczinski discloses a node controller, wherein the XOR operation is used to calculate a parity data for writing a full or a partial RAID stripe(Column 5, Lines 35-38).

33. Regarding claim 27, Styczinski discloses a node controller, wherein the XOR operation is used to reconstruct a lost data using a parity(Column 5, Lines 35-38).

Response to Arguments

34. Applicant's arguments filed March 18, 2004 have been fully considered but they are not persuasive. Applicant argues that although Cohen discloses the memory controller using

combinational logic, Cohen does not disclose performing a logic operation on data. However, Cohen discloses the use of an address comparator(Figure 3, 56), which is well known in the art to perform logic operations on data, as evidenced by Malinowski('441).

Conclusion

35. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nimesh G Patel whose telephone number is 703-305-7583. The examiner can normally be reached on M-F, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-2100.

Nimesh G Patel
Examiner
Art Unit 2112

NP NP
May 19, 2004

Glenn A. Auve
Primary Patent Examiner
Technology Center 2100